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PATENT APPLICATION

TRANSCONDUCTANCE DEVICE EMPLOYING NATIVE MOS TRANSISTORS

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TRANSCONDUCTANCE DEVICE EMPLOYING NATIVE MOS TRANSISTORS

BACKGROUND OF THE INVENTION

This invention relates generally to electrical systems which are integrated in a semiconductor chip, and more particularly the invention relates to systems for signal processing such as telecommunications systems and to gyrator filter elements and transconductance devices used therein.

Fig. 1 is a functional block diagram of a wireless receiver for recovering transmitted data. Typically, the receiver includes an antenna 10, filter 12, balan 14, impedance matching network 16, and low noise amplifier 18 for receiving and preparing a signal at a transmission frequency for a frequency down converter shown generally at 20. Down converter 20 includes phase quadrature mixers 21, 22 driven by a phase lock loop synthesizer 23 which reduce the frequency of the received signal and pass the phase quadrature mixer outputs to low pass frequency filters 24, 25. The filtered signals are then passed to mixers 26, 27 which step the filtered signals to an intermediate frequency (IF) for further processing and signal recovery by demodulation of the IF signal as assumed at 28.

The system of Fig. 1 is a fabricated in a single semiconductor chip as an integrated system on a chip. An operating standard, known as Bluetooth, has been established for wireless telecommunications systems on a chip which has stringent operating requirements as illustrated in Figs. 2A, 2B. The maximum usable signal level the receiver shall operate at will be better than –20dBm and the reference sensitivity level referred to is -70dBm.

The charts of Figs. 2A, 2B show the two-tone requirements for Bluetooth compliance. The reference sensitivity performance, which is a Bit Error Rate (BER) + 0.1%, shall be met with a wanted signal at a frequency f_0 with a power level 6db over the reference sensitivity level in the presence of the following: A –39dBm signal at f1 and a Bluetooth modulated signal at f2 of –39dBm, where f0, f1, and f2 are defined as f0=2f1-f2 and f2–f1 = n*1mhz, where n can be 3, 4 or 5. System simulations have shown that to achieve a BER of less than 0.1% requires a signal to noise ratio of 20db (worst case), thus to be Bluetooth compliant in the presence of out of band blockers, the third order in a modulation shall be -64-20dBm=-84dBm.

System simulations have shown that channel selection of a Bluetooth signal in the presence of adjacent channel blockers, with powers not exceeding –39dBM, can be achieved using a fc accuracy of better than 5%.

Filter elements in the system require inductive elements such as shown in Fig. 3A. Since inductors are difficult to realize in integrated circuits and systems, a functional equivalent inductive element, or gyrator, has been devised. As shown in Fig. 3B, the gyrator comprises variable transconductance elements, GM, serially connected with a shunt compacitance, C.

Fig. 4 is a schematic of a known transconductance cell such as discussed Schaumann, simulating Lossless ladders with Transconductance – C Circuits, IEEE Transactions on Circuits and Systems II, Analog and Digital Signal Processing, March 1998, pages 407-410; and Johns and Martin, Analog Integrated Circuit Design, John Wiley and Sons, Inc., 1997, pp 597-600. These prior art references discuss the use of CMOS transconductance using triode (MOS) transistors.

A problem with the use of the known transconductance cell lies in adverse effects of source-bulk voltage (VSB) on MOS transistors used in the transconductance cell. Variations in VSB due to bulk (chip) stray voltages can adversely affect transconductance. Further, control voltage in a gyrator can have a limited dynamic range when using conventional MOS transistors.

BRIEF SUMMARY OF THE INVENTION

In accordance with the invention a transconductance element or cell in a system on a chip or other integrated circuit has improved response to noise in a semiconductor chip arising from extraneous signals propagated from analog and digital circuitry within the system.

A feature of the invention is the use of native transistors in the transconductance cell. The native MOS transistor has a lower threshold voltage V_t than the conventional MOS transistor, which leads to lower variation of GM due to source to bulk voltage variations.

In one embodiment, a ring oscillator employing cross-coupled transconductance devices generates a control voltage, V_c, which controls transconductance devices in low pass filters and achieves more accurate control of the filter cutoff frequencies. The system has reduced substrate noise susceptibility via VSB variations. The reduction in

transconductance variation is particularly applicable with low supply voltage constraints of present and future systems on a chip.

The invention and objections and features thereof will be more readily apparent from the following detailed description and appended claims when taken with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a functional block diagram of a conventional wireless receiver.

Figs. 2A, 2B are frequency charts illustrating Bluetooth system requirements.

Figs. 3A, 3B illustrate filter elements using inductive elements and transconductance devices, respectively.

Fig. 4 is a schematic of a known transconductance cell as used in the filter of Fig. 3B.

Fig. 5 is a schematic of a ring oscillator which generates a control voltage, V_c.

Fig. 6 is a schematic of a voltage controlled oscillator for use in the ring oscillator of Fig. 5 and comprising cross coupled transconductance cells.

Figs. 7A, 7B illustrate transconductance variation with varying VSB for a native transistor and for a standard MOS transistor, respectively.

Figs. 8A-8D are graphs illustrating current linearity and V_c dynamic range for a transconductance cell with normal MOS transistors and with native MOS transistors.

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DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

Fig. 5 is a functional block diagram of a ring oscillator which generates a control voltage, V_c, for controlling low pass filters 24, 25 in Fig. 1. The ring oscillator includes a voltage controlled oscillator 42 in a phase lock loop including a phase/frequency detector 44 which receives the output of Vco 42 and compares the output with a reference frequency from crystal oscillator 46. The phase and frequency difference detected by detector 44 is applied to a charge pump 48 which generates a voltage for controlling Vco 42. The voltage from charge pump 48 is the control voltage, V_c, which is also applied to control transconductance devices in low pass filters 24, 25.

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Fig. 6 is a schematic of Vco 42 implemented as a second order harmonic oscillator including cross coupled transconductance cells 52, 54, and capacitors 53, 55 and a non-linear resistor 56. As noted above, the control voltage generated by ring oscillator of Fig. 5 is used to control the transconductance, GM, stages within the filter and hence the cutoff frequency of filters 24, 25. Each transconductance cell or GM stage can be identical to

the transconductance cell shown in Fig. 4. The circled transistor devices shown at 60 in Fig. 4 function as load resistors for current sources 62, 64 which are serially connected with current sources 63, 65 to provide two outputs Out P and Out N of the transconductance device. Block 66 is a voltage common mode feedback for the current sources, the details of which are known and not described further herein.

Within each transconductance (GM) cell the circled device 60 is used to control the transconductance according to the equation:

$$Gm=\mu\ Cox\ (W/L)\ (Vgs-Vt) \qquad \textbf{Equation 1}$$

Where μ is the surface mobility of the channel (cm^2 /volt),

Cox is the capacitance per unit area of the gate oxide (F/ $cm^{2)}$,

W is the effective channel width of the circled device,

L is the effective channel length of the circled device,

Vgs is the gate to source voltage, and Vt is the threshold voltage of the circled device. With the PLL tuning scheme it is possible to achieve the 5% frequency tolerance, however this does not take account of noise picked up through the substrate. This noise can severely degrade the performance of the filter within a SOC environment and it is the topic of this patent to improve this. Referring to Equation 1, it is clear that a source of degradation to GM is via the threshold voltage Vt. It is prudent, therefore to examine Vt more closely. The threshold voltage for an n-channel transistor is given by:

$$Vt=Vt0+\gamma((\sqrt{2}|\varphi F|+VSB)- +(\sqrt{2}|\varphi F|)) \qquad \textbf{Equation 2}$$

Where Vt0 Vt(VSB=0),

γ Is the bulk threshold parameter ($\sqrt{}$volts)

φF is the strong inversion surface potential (volts)

VSB is the source to Bulk Voltage.

It is clear from this equation that any injection of noise between the transistor source and the semiconductor chip bulk will cause a variation in Vt and hence GM. This VSB can easily arise if the source and bulk are not tied down at exactly the same potential. Forcing VSB to be zero throughout the filter can be very difficult to do and an alternative approach is presented herein.

As noted from Equation 1, the threshold voltage, V_t, of the MOS transistors affects the transconductance. In accordance with the invention the use of a low to zero threshold voltage transistor, a "native" device, improves the filter performance in the presence of substrate noise. As is well known in the semiconductor art, a "native" transistor

does not have threshold adjusting dopants in the channel region as in conventional MOS transistors. The V_t of a native device used with the transconductance cell of Fig. 4 is a 0.041 volt has a saturation current, I_{sat} of 5.83 mA. Although the V_t of the native device has a similar dependence on VSB as does the conventional MOS transistor, its low absolute value with respect to a Vgs of approximately 500 mV, means that the overall transconductance does not vary much with VSB. Figs. 7A, 7B illustrate transconductance variance with varying VSB with a native transistor load and with a standard MOS transistor load, respectively. Fig. 7B is the small signal transconductance variance due to ± 100 mV VSB using a standard MOS arrangement, whereas Fig. 7A is GM variance using the native MOS transistor. It is noted that the native MOS transistor provides a variance of ± 0.3% up to 1 MHz, whereas the standard MOS transistor has a variance of ± 9.7% over the same frequency range.

Another advantage using the native MOS transistor is that the control voltage has more dynamic range, as illustrated in Figs. 8A-8D. Figs. 8C and 8D illustrate transconductance variance for a given V_c. It is clear that the slope or GM gain has changed with the native device without changing the maximum or minimum transconductance values. These plots illustrate that the native transistor devices offer the advantages of providing a sufficiently wide range of transconductance values as the process shrinks and supply voltage, V_{dd} is reduced. Further, the native MOS device has a lower transconductance gain with respect to the transconductance control voltage V_c thus resulting in less jitter of the phase lock lock used to tune the filter, and hence a more stable loop control voltage. Accordingly, a signal processing system on a chip fabricated with transconductance devices employing native MOS transistors as described can have more accurately controlled cutoff frequencies with reduced substrate noise susceptibility via the VSB voltage. The slope of transconductance versus control voltage is reduced and provides a lower jitter phase lock loop for use in filter tuning. The provision for transconductance variance is particularly applicable to low voltage supply constraints as is being encountered now and anticipated to be more so in the future.

While the invention has been described with reference to specific embodiments, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.